

Triggers and metastability

- 1 Asynchronous triggers
- 2 Synchronous triggers
 - 2.1 Level control trigger
 - 2.2 Edge control trigger
- 3 Other types of triggers
- 4 Transformation of triggers
- 5 Initial state setting and trigger blocking
- 6 Metastability of triggers
- 7 Double sampler

Triggers and metastability

Triggers are the simplest **sequential** components. We distinguish **asynchronous** trigger circuits which respond to activity of the input signals immediately, and **synchronous** triggers, which respond to coincident activity of input signals and synchronizing (clock) pulses.

The simplest circuit is created by connecting two inverters in a circle. It thus creates a positive feedback loop. The oscillation in this case does not occur, since the feedback circuit takes one of the two possible stable states. The circuit is therefore called **bistable**. Fig. 1 on the left shows the connection of two gates in a circle, the figure in the middle the same connection, just redrawn into a more common shape. The figure on the right shows the effect of the feedback.

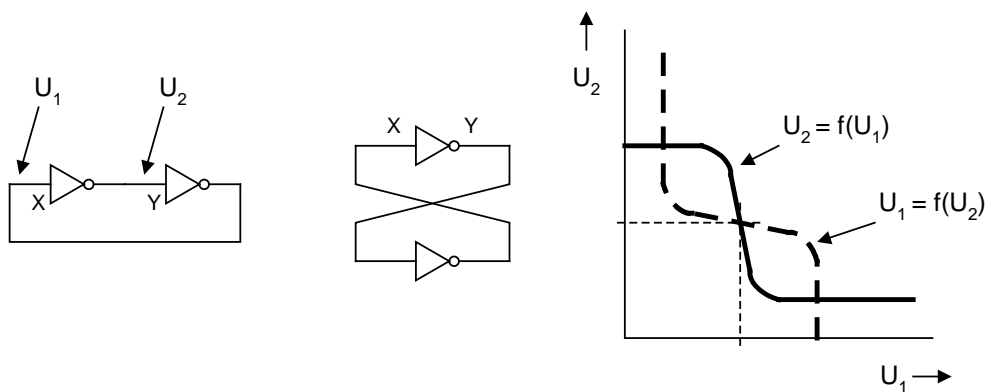


Fig. 1: Trigger principle

The voltage U_1 at point X causes the voltage U_2 at point Y. The relationship is given by the transfer characteristic $U_2 = f(U_1)$, shown by a solid thick line. Conversely, the voltage U_2 at point Y causes the voltage U_1 at point X. The relationship is given by the transfer characteristic $U_1 = f(U_2)$, shown by the dashed thick line. When the voltage U_1 or U_2 diverts beyond the point marked by dashed coordinates, the circuit changes state - flips over. If the deviation is below this point, the circuit returns to the initial state. The question is what happens when the deviation reaches to the intersection of the two characteristics. The trigger circuit enters an abnormal state called the **metastable** state. Metastability is covered in further text in this chapter.

In the described simple version it is necessary to apply a certain voltage to the input X or Y in order to change the state of the circuit. However, inputs X and Y are connected with the outputs of the inverters. Therefore, current is also required for changing state, even if only as a **short** pulse. Short because at the output of the opposite gate the state changes with a delay $2 \cdot t_{pd}$ and it will then be identical with the state at the input X - at that moment the current stops flowing.

The circuit from Fig. 1 is commonly used in static semiconductor memories for its simplicity. It is also used in active terminators (see chapter Three-state outputs and open collectors) just for pulse current consumption when the state changes.

1 Asynchronous triggers

Other inputs of gates can also be used to control the trigger, as shown in Fig. 2 for the case of NOR gates - on the left is a schematic symbol, in the middle the connection with logic gates, on the right is a truth table.

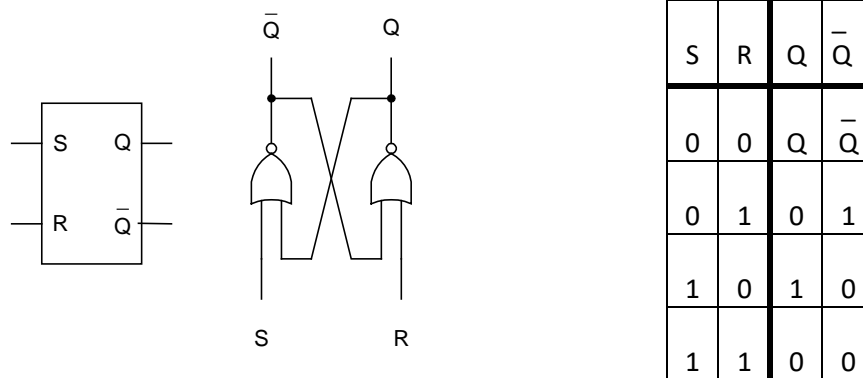


Fig. 2: Trigger with NOR gates

If state 0 is on both inputs R and S, the passage of the signal through the feedback loop is not blocked in any way and the circuit will be permanently in one of two stable states. With $S = 1$ it is always $\bar{Q} = 0$ and if also $R = 0$, then $Q = 1$. Due to the symmetry of the circuit, in the opposite situation on the inputs (i.e. $S = 0$ and $R = 1$), then on the outputs is $Q = 0$ and $\bar{Q} = 1$. The truth table is in the picture on the right.

The first line documents the **memory** property of the trigger - constant value remains at the Q output, as well as at the output \bar{Q} . The second line is a **resetting**, and the third line **setting** of the output Q . According to the last line, it is obvious that when $R = S = 1$, both outputs must be at 0. While this is contradictory, because Q cannot be equal to \bar{Q} , a simple renaming of the signals would resolve the formal problem. However, the problem is in the **transition** from the input state $R = S = 1$ to the state $R = S = 0$. When $R = S = 1$, the trigger is put into a symmetrical state - both its gates have the same voltage at the inputs and outputs. After the **simultaneous** change of both R and S from 1 to 0, the resulting state is **random** due to the random non-symmetry of the two gates. The input state $R = S = 1$ is sometimes considered a forbidden state, which is not correct - prohibited is the **transition** from $R = S = 1$ to $R = S = 0$. All other transitions are completely without problems. The trigger described above is called an **RS circuit**.

The trigger circuit RS can also be assembled from NAND gates, as shown in Fig. 3. When $\bar{R} = \bar{S} = 1$, the circuit remembers its state. At $\bar{S} = 0$ and $\bar{R} = 1$ is $Q = 1$, and at $\bar{S} = 1$ and $\bar{R} = 0$ is $Q = 0$. The inputs $\bar{S} = \bar{R} = 0$ cause a symmetric state $Q = \bar{Q} = 1$ and the **transition** to $\bar{S} = \bar{R} = 1$ is **prohibited**.

There are other types of asynchronous triggers, but these are less common than those described above.

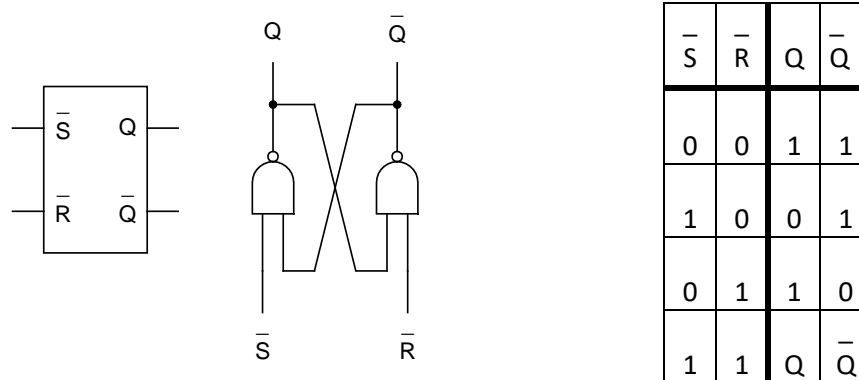


Fig. 3: Trigger RS with NAND gates

2 Synchronous triggers

2.1 Level controlled trigger

Trigger circuit D (see figure 4) is, in contrast to the previous circuits RS, **synchronous**, because it changes the state only in the interaction of input signal D and synchronization or **clock pulse** CLK . During the clock signal $CLK = 1$ is $S = D$, and $R = \bar{D}$ and therefore $Q = D$. After the end of the clock pulse, when $CLK = 0$, is $R = S = 0$. This is a combination of values at which the trigger RS with NOR gates does not change state. The state reached during the clock pulse is thus captured. Trigger with this kind of management is called **level controlled** or shortly "**latch**". The operation of this circuit is clear, but complications occur if input D changes with the end of the CLK pulse. As the result, it is not clear what state will be captured. This situation is one of the manifestations of **metastability** and should be avoided.

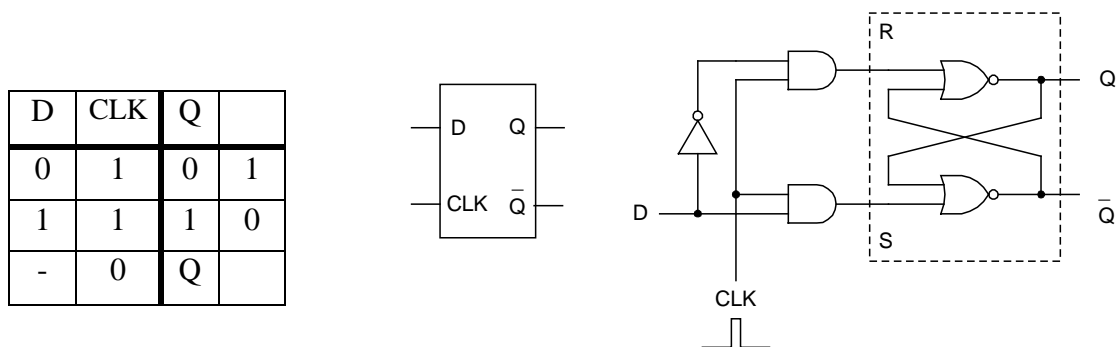


Fig. 4: Truth table, schematic symbol and schematics of the level controlled trigger

The "-" symbol in the table indicates arbitrary value 0 or 1.

Synchronous KO type D can be realized by an even simpler connection using CMOS **switches** - see Fig. 5 (switches are marked symbolically). The CLK pulses control both switches in antiphase. When S_2 is ON and S_1 is OFF, there is a strong positive feedback that will bring the circuit to one of two possible steady states: $X = 1, Y = 0$ or $X = 0, Y = 1$. The D signal is not applied. Conversely, when S_1 is on and S_2 is off, the feedback is interrupted and the state at outputs X and Y is given by the state at input D ($X = \bar{D}, Y = D$).

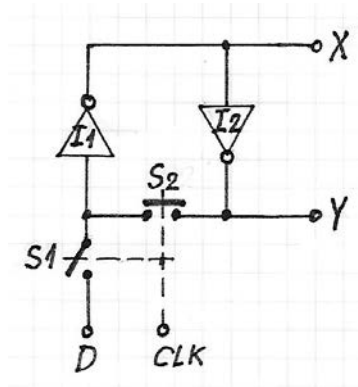


Fig. 5: Principle of synchronous trigger D with switches

Now suppose the change of the CLK from 1 to 0, when S_1 has been switched ON and is just switching OFF (S_2 is switching ON) and at the same time the signal changes at D. Both inverters are only partially diverted, about halfway between U_H and U_L , input D is disconnected (S_1) and the feedback is closed (S_2). The trigger is now partially diverted and "left to itself". The next course will depend on the extent to which the circuit has been diverted by the input. Again situation leads to **metastability**.

The trigger of Fig. 5 is preferred over that of Fig. 4. Simple analysis of the prices in numbers of transistors yields number 18 for Fig. 4 and number 8 for Fig. 5 - the clear case.

The following Figure 6 is a timing diagram valid for all **level controlled** triggers.

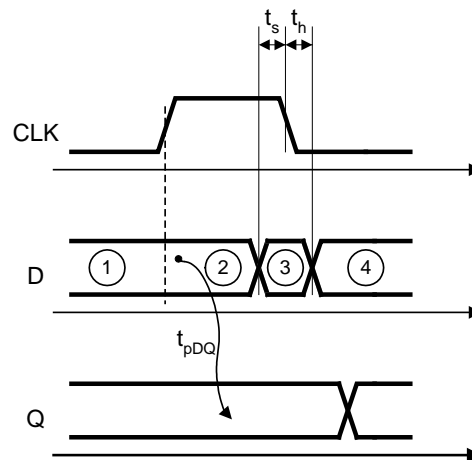


Fig. 6: Timing diagram of level controlled triggers

In area 1, input changes have no effect, in area 2 (during CLK) they are transmitted to the output with a delay t_{pDQ} , in area 3 changes are prohibited and in area 4 again input changes have no effect. Important is the time t_s - **setup time** and t_h - **hold time**. These times define the area in which the input state must not change; otherwise a metastable state may arise. By keeping the setup and hold time, it is guaranteed that the last change in the input will properly affect the output, which will then remain constant until the next clock pulse.

The basic features of a level-controlled trigger are:

- In the course of the clock pulse, the circuit is transparent for the input signal - it passes the input signal to the output.
- After the end of the clock pulse, the last state at the output is retained.
- The input signal must not be changed in the area around the falling edge of the clock pulse.

*Asynchronous and **level controlled** triggers are also called "**latches**".*

2.2 Edge controlled trigger

Another way to control the trigger is the **edge control**. The timing diagram is shown in Fig. 7.

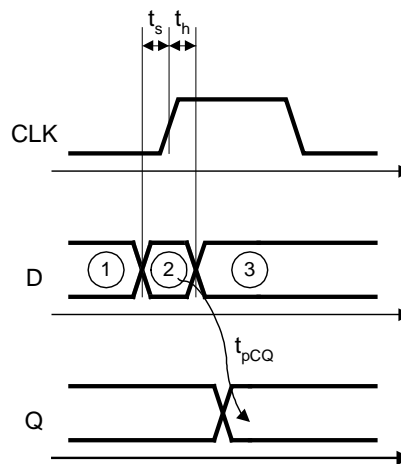
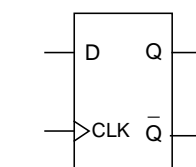


Fig. 7: Timing diagram of edge controlled trigger

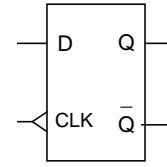
Input changes in areas 1 and 3 are not reflected in the output. The state at the input in area 2 is transferred to the output with a delay t_{pCQ} after the leading edge CLK. The input state **must not change** during the period from t_s to t_h around the **rising** edge of CLK.

In the truth table of the flip-flop circuit controlled by the rising edge in Fig. 8, this edge is indicated by the arrow \uparrow , in the schematic symbol by the arrow inside the circuit. Similarly exists also **falling edge** control; the table and time diagrams are valid for them after the exchange of CLK for \overline{CLK} and \uparrow for \downarrow . In the following text, we will use the designation **active edge** for the clock edge that causes a change of state on the output.

D	CLK	Q	\overline{Q}
0	\uparrow	0	1
1	\uparrow	1	0
-	0	Q	\overline{Q}
-	1	Q	\overline{Q}
-	\downarrow	Q	\overline{Q}



rising-edge controlled



falling-edge controlled

Fig. 8: Truth table and schematic symbols of edge-controlled triggers

An edge-controlled trigger is **more complex** than a level-controlled one. There are two basic methods for achieving an edge response:

- CLK pulse edge detection
- Master-Slave connection

The principle is shown in Fig. 9. The edge detector consists of an AND gate and an inverter, which serves as a delay circuit. The length of the Z pulse is approximately equal to t_{pd} of the inverter. The pulse can be extended by inserting a larger number of inverters in series (always an odd number).

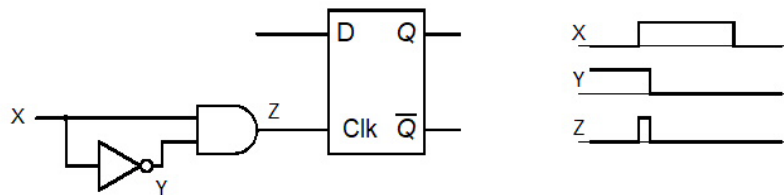


Fig. 9: Edge control with an edge detector

The second and more frequent version uses a pair of level controlled triggers in the Master-Slave connection - see Fig. 10. The clock pulses are mutually inverted. During $CLK = 1$, M is open for changes at the input, but due to the reverse phase, S is blocked, so that its state and the output Q do not change. Only when $CLK = 0$ is the state of M passed to S. The internal state of M is therefore being set for the **entire duration** of $CLK = 1$, but is **visible** at the output only at $CLK = 0$. From the external point of view, the trigger MS behaves similarly to that controlled by CLK edge - in this case **falling** edge at which the output value changes.

As in Fig. 6, the first trigger could reach metastability during $CLK = \downarrow$, if the change of the input took place in the marked window - the metastability would then be reflected in the output Q_2 .

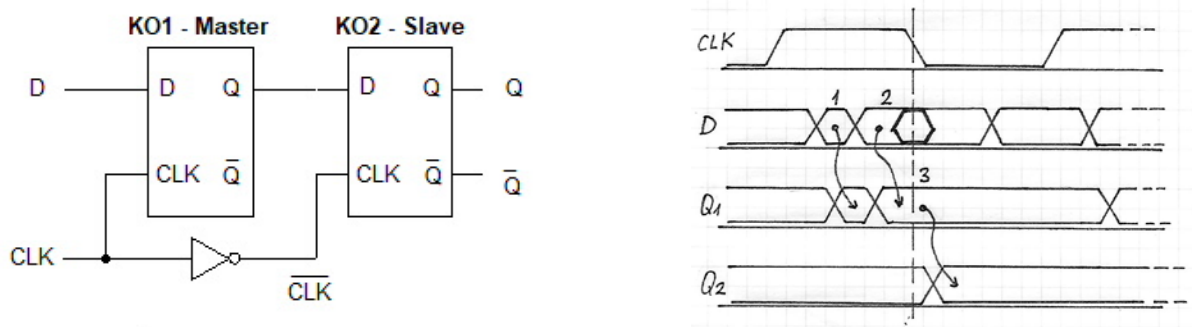


Fig. 10: Master-Slave trigger

For large integration circuits, where there are a large number of triggers, their simple design is important. This is achieved by two-phase triggers MS, where the clock pulses are introduced in two phases, i.e. CLK and \overline{CLK} . This saves one inverter in each trigger.

For the correct operation of the flip-flop circuit with edge control, it is necessary to observe some dynamic parameters of the input signals. First of all, it is the **setup time** and the **hold time**. Furthermore, it is the minimum **steepness** of the clock pulse edge, the minimum **duration** of the clock pulse in state 1 and in state 0. Failure to comply with any of these

conditions can cause unreliable operation or a **metastable** condition where the resulting state is accidental.

The basic features of an edge-controlled trigger are:

- The decisive factor is the state at the inputs in the immediate vicinity of the active edge of the clock pulse.
- At other times, the changes in the inputs are insignificant.
- Improper timing of clock pulses and input signals can cause metastability.

Edge controlled triggers are also called "flip-flops".

To illustrate the **time parameters**, the values of a typical synchronous trigger circuit for surface mounting are given. In the case of a circuit integrated on the chip the values are at least one or two orders of magnitude lower.

$t_W \geq 5 \text{ ns}$... clock pulse length
 $f_{CLK} \leq 160 \text{ MHz}$... clock frequency
 $t_s \geq 5 \text{ ns}$... setup time
 $t_h \geq 0$... hold time
 $t_{pCQ} = 6.3 \dots 8.8 \text{ ns}$... output delay time after the CLK edge
 $\Delta t / \Delta U \leq 20 \text{ ns/V}$... minimum slope of the CLK edge

3 Other types of triggers

Another type of a trigger is the **T-trigger**. It exists in two variants - asynchronous and synchronous (see Fig. 11). An **asynchronous T-circuit** with each active edge at the T input alternates state - **toggles**. A **synchronous T-circuit** alternates state with each active edge of CLK , but only when $T = 1$. At $T = 0$, it maintains its state. T-triggers are very common.

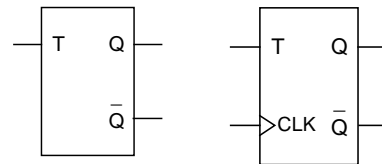


Fig. 11: Schematic symbol of the T-trigger, left T asynchronous, right T synchronous

Very universal, although not very common, is the **JK-trigger** - see Fig. 12. With the exception of the 4th line, its truth table coincides with the table of RS-trigger with NOR gates (Fig.2). When $J = K = 1$, the circuit alternates state. Therefore, the transition from $J = K = 1$ to $J = K = 0$ is without problems here.

J	K	Q	\bar{Q}
0	0	Q	\bar{Q}
1	0	1	0
0	1	0	1
1	1	\bar{Q}	Q

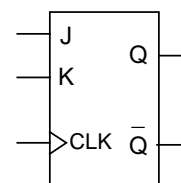


Fig. 12: Truth table and schematic symbol of the JK-trigger

The fourth line is also the reason why the JK-trigger **cannot** be level controlled, but must be edge controlled. At $J = K = 1$ the circuit changes state and with level control it would change state for the entire duration of $CLK = 1$, so it would actually oscillate. This, of course, is not permissible.

4 Transformation of triggers

A trigger of one type can be converted - transformed - into a trigger of another type. The basis is an edge controlled **D-trigger**. The first case is the transformation of D to **asynchronous T** (see Fig. 13). At input D , the state is opposite to that at output Q , so the next clock pulse will turn the circuit to the opposite state.

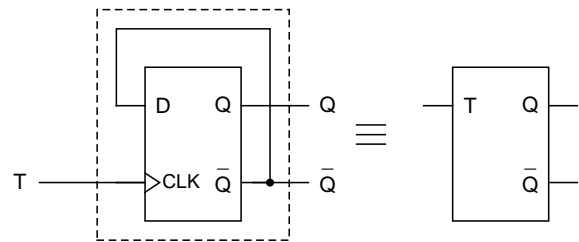


Fig. 13: Transformation of a D-trigger to an asynchronous T-trigger

Another case is the synchronous **D to T** transformation (see Fig. 14). If $T = 0$, the XOR circuit does not change Q and the state of the circuit does not change. When $T = 1$, the XOR inverts Q and the circuit alternates its state.

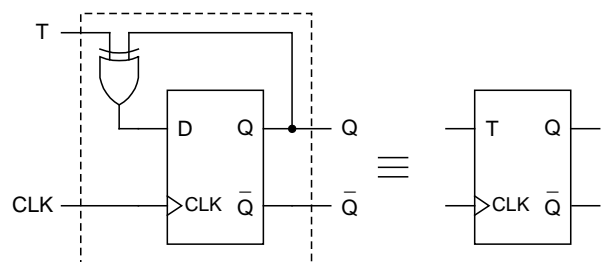


Fig. 14: Transformation of a D-trigger to a synchronous T-trigger

The circuit in Figure 15 is universal and can operate as **D** or **synchronous T**. It is used in programmable circuits. If type D is requested, then $X = 0$ and XOR does not change the input signal T/D - the circuit works as type **D**. If type T is requested, then $X = Q$ and the case indicated in the previous figure occurs - the circuit works as type **T**.

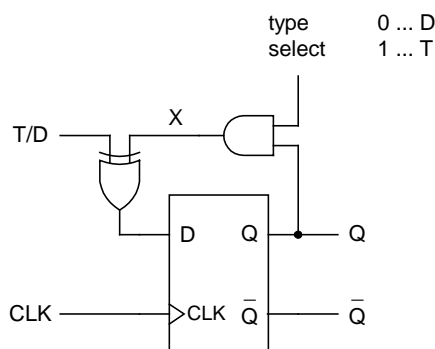


Fig. 15: Universal D/T trigger

Finally, Fig. 16 shows the transformation of **D to JK** trigger.

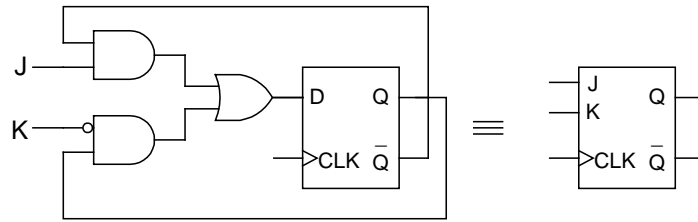


Fig. 16: Transformation of a D-trigger to a synchronous JK-trigger

5 Initial state setting and trigger blocking

Very often it is necessary to ensure a defined initial state of the trigger after the start-up of the power supply, or also during the operation of the system. Fig. 17 shows the variants. The figure on the left uses the **reset** input, or the **set** and reset inputs that some triggers have. These are always effective, regardless of other inputs - compare with Fig. 3. Combination $\overline{R} = \overline{S} = 0$ can lead to an **undefined** state. Figure 17 in the middle shows the use of these inputs to allow resetting (input CLR) and preloading data (input DATA) under the control of the LD command. This requires the addition of simple logic circuits (in a dashed box). Both CLR and LD take precedence over CLK.

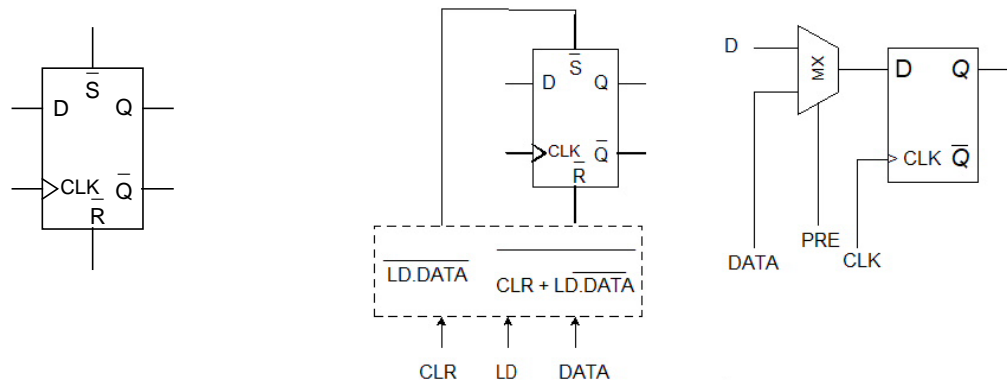


Fig. 17: Setting the initial state of the trigger

In Figure 17 on the right, a **multiplexer** is used. The PRE signal determines whether the trigger will function normally or whether the initial data will be loaded in it. To do this, however, it is necessary to switch the MX at the right time in relation to the CLK in order to meet the conditions for timing the trigger's signals.

The operation of flip-flops must sometimes be **blocked** and again **re-enabled**. However, this cannot be realized in the manner according to Fig. 18 on the left, where the supply of clock pulses to the trigger is simply interrupted. Distribution nets of synchronization pulses are usually very demanding and sensitive parts of every synchronous system with strict requirements on signals delay. Inserting additional devices into this net is completely **undesirable**.



Fig. 18: Blocking the operation of the trigger

A suitable solution is shown in Figure 18 on the right. This is not a blocking of the clock pulse, but an appropriate switching of the input signal D . When $EN = 1$, the trigger works normally; when $EN = 0$, $D = Q$ and the trigger will not change state - it is effectively blocked. The CLK net is not affected in any way. The timing of the EN signal must comply with the conditions for the **timing** of the trigger signals.

6 Metastability of triggers

Metastability is an undesirable phenomenon related to the operation of triggers. It results in an unpredictable state at the outputs, which is of course completely undesirable. The primary cause of metastability is the existence of positive feedback in the circuit - but the trigger is based on that and cannot function without it. Metastability manifests itself in several ways:

1. The trigger toggles partially, but returns after a certain time.
2. The trigger is only partially toggled and after a certain time it continues until it is toggled completely.
3. The trigger partially toggles and remains in this equilibrium state indefinitely.

The last case is theoretical, but points to the upper limit for considerations of the length of the **metastability time** t_{met} , which is an important parameter. It is defined as the time that the trigger needs to stabilize the state **after** the normal delay time t_{pCQ} . Stabilization of the state is given by reaching one of the prescribed output voltage levels U_{Hmin} or U_{Lmax} . Time t_{met} is not constant and depends on the moment of change of the input signal with respect to the change of CLK .

Metastability occurs in **all types** of triggers, both asynchronous and synchronous. The case of a simple trigger type RS is shown in Fig. 19. It is obvious that the symmetrical state 0,0 at the outputs causes a problem only with the **simultaneous** transition to R and S from 1,1 to 0,0. As can be seen, the state at output Q stabilizes after some time, but it can be 0 or 1.

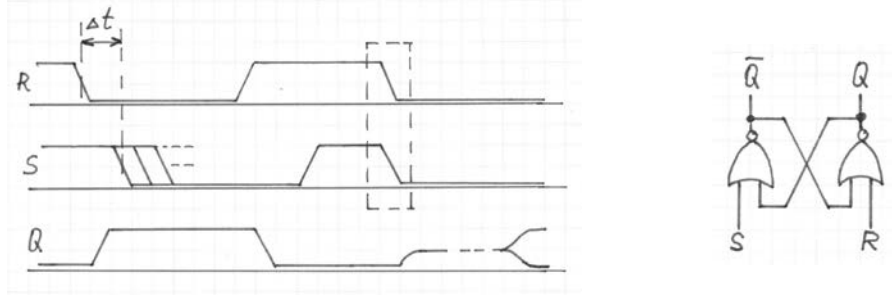


Fig. 19: Metastability in RS trigger

Conditions for the formation of metastability are shown in Fig. 6 and 7. In level control is problematic the **end** of clock signal simultaneously with the change of input; in edge control the **active edge** of CLK simultaneously with the input change.

Metastability can be prevented by appropriate **timing** of the signals at the inputs of the triggers. To do this, it is necessary to perform a very accurate analysis of the **delay** of individual signals, both data and synchronization. Delays occur both in the components and in the **connections**. The quality of signals, especially jitter, also plays a role. The delay in the connections can only be known when the complete layout of the circuit is known. Computer aided design is necessary.

Good knowledge of metastability requires the existence of a mathematical description from which important conclusions can be drawn. Important information is the **probability** of metastability and its duration. At the outset of the considerations, it should be emphasized that metastability is of a statistical nature due to the random course of trigger toggling.

Theoretical analysis of the duration of the metastable state, supported by experimental measurements, leads to the relationship

$$P(t_{met} > t) = \frac{K_1}{T_{CLK}} e^{-K_2 \cdot t} \quad (1)$$

where $P(t_{met} > t)$ is the probability that the metastability will last longer than the time t , K_1 and K_2 are the parameters of the given trigger (depending on the technology) and T_{CLK} is the period of clock pulses.

The probability of the occurrence of metastability is given by the probability that the state change at the trigger input will occur at the time of the **metastable window** $T_O = t_s + t_h$. This probability is given by the ratio T_O/T_{CLK} , where T_{CLK} is the period of the clock pulses. It is assumed that the data changes are not synchronized with the clock pulses in any way and can therefore occur at **any time**. The frequency of data changes (i.e. the number of changes per second) at the trigger input is denoted as N_D - each change is calculated, i.e. both $0 \rightarrow 1$ and $1 \rightarrow 0$. The number of metastability events per second N_M will therefore be on average

$$N_M = N_D \cdot T_O / T_{CLK} \quad (2)$$

7 Double sampler

Obviously, if the trigger input is not synchronous with the CLK , metastability **must** occur from time to time and in principle cannot be avoided. However, there is the possibility to make metastability "invisible" by a suitable circuit design. The solution is called **double sampler** or **synchronizer**. The principle is shown in Fig. 20 and consists in the inclusion of two consecutive triggers. With the first CLK , the state at D_1 will be shifted to Q_1 . With the second CLK , the state at $Q_1 (= D_2)$ will be shifted to Q_2 . If Q_1 gets in metastability which ends **before** the second CLK , then Q_2 toggles without the risk of metastability state. This way the events at Q_1 will be "invisible" for other circuits and the metastability does not propagate further.

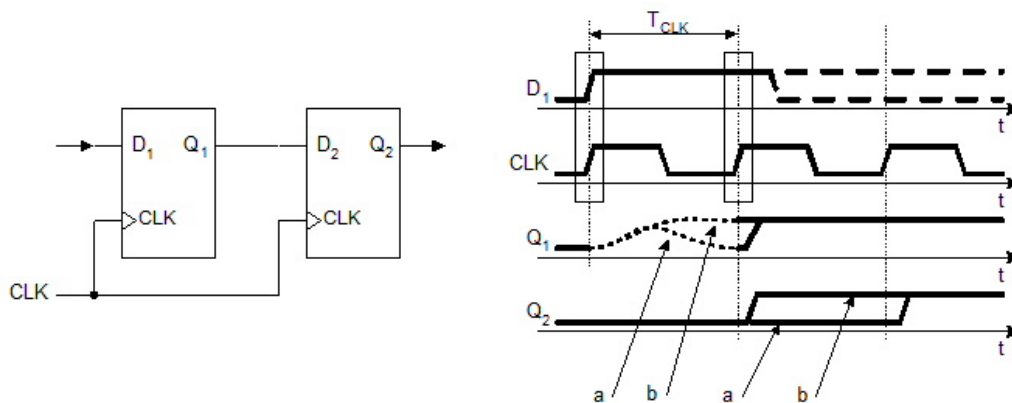


Fig. 20: Double sampler

The timing diagram in Fig. 20 shows two possible situations. If at the end of the metastable state the trigger Q_1 toggles correctly (e.g. from 0 to 1 as shown in the figure), then Q_2 also toggles correctly (to 1 - waveform *b*). If, however, Q_1 incorrectly toggles to 0 and the data at input D_1 still holds, then the first trigger toggles to 1 with the second pulse CLK and the second trigger toggles still later after another tact of CLK (waveform *a*). The signal at Q_2 is always correct, but with possible additional tact of delay. Therefore, an **uncertainty of 1 CLK cycle** always exists.

From Fig 20 it is further evident that in order to capture every change of the input signal (with a possible uncertainty of one cycle, as explained), both the state 0 and the state 1 at the input must last at least one CLK period. This means the input signal period must be longer than twice the CLK period - in other words, the sampling frequency must be **at least twice** the input signal frequency. This is an interesting result that testifies to the broad validity of Shannon's sampling theorem.

A problem may occur if the metastable state Q_1 does not end until the next CLK , so that Q_2 also gets into metastability. Therefore, it is important to know the metastability time t_{met} . However, this is a random value, so the only information is the **probability** of metastability duration.

The formula which evaluates the **mean time between failures (MTBF)** of the double sampler is following:

$$MTBF = \frac{T_{CLK} e^{K_2(T_{CLK} - t_s)}}{N_D K_1} \quad (3)$$

where K_1 and K_2 are parameters of the trigger, specified by the manufacturer of the trigger or more complex components containing triggers - e.g. programmable logic devices. N_D is the frequency of changes at the data input.

Obviously, the $MTBF$ increases exponentially with the period of clock impulses. This is the main parameter that needs to be calculated to achieve the required reliability.

It is clear that the $MTBF$ increases exponentially with the **period of** clock pulses. This is the main parameter that must be calculated to achieve the required reliability. Of course, other values can be calculated from relation (3).

Improving $MTBF$ by reducing the CLK frequency is effective, but it reduces the overall system speed, since clock pulses also work in other circuits. Then it is possible to place another trigger behind the double sampler - this way a **triple sampler** is obtained. The $MTBF$ of the sampler composed of the first and second trigger is then multiplied by the $MTBF$ of the sampler composed of the second and third trigger - this way we get $MTBF^2$. This is usually a sufficiently large number even if the CLK frequency is not reduced.

In any case, we treat statistical data, and even the very low probability of failure (large $MTBF$) does not mean that the failure cannot occur immediately at the next moment (and another failure after a million years later).

High **reliability** (high $MTBF$) and high **safety** must be distinguished. While reliability means low probability of failure, safety means ensuring that the possible failure does not cause danger to people or to things. This requires special methods of the design of safe systems, which anticipates the possibility of failure.

Example:

We have a double sampler with triggers' parameters:

$$\begin{aligned} K_1 &= 0,15 \cdot 10^{-9} \\ K_2 &= 5,11 \cdot 10^9 \\ t_s &= 500 \text{ ps} = 0,5 \cdot 10^{-9} \text{ s} \end{aligned}$$

The sampler operates with the frequency $f_{CLK} = \mathbf{333 \text{ MHz}}$, tj. $T_{CLK} = 3 \text{ ns} = 3 \cdot 10^{-9} \text{ s}$. The data changes on average once every 5 seconds, i.e. $N_D = 0.2 \text{ Hz}$. Calculate the $MTBF$ of the sampler, the requirement is at least 10 years.

1. After substituting into relation (3) we get $MTBF \approx 3,5 \cdot 10^7 \text{ s}$, which is about **1.1 years**.

That is not a sufficient result. Next we choose $f_{CLK} = \mathbf{250 \text{ MHz}}$, i.e. $T_{CLK} = 4 \text{ ns} = 4 \cdot 10^{-9} \text{ s}$.

2. After substituting into relation (3) we get $MTBF \approx 7.8 \cdot 10^9$, which is about **247 years**.

That is already an acceptable result. For extreme reliability we will try $f_{CLK} = 200 \text{ MHz}$, i.e. $T_{CLK} = 5 \text{ ns} = 5 \cdot 10^{-9} \text{ s}$.

3. After substituting into relation (3) we get $MTBF \approx 16.1 \cdot 10^{11}$, which is about **51 thousand years**.

The significant influence of the **exponential** in the numerator of relation (3) is obvious. However, it is also clear that such a favorable result follows from a very low frequency of **changes** in the input. If the data change at least approximately comparable to clock pulses, the situation would be worse. For example, when increasing N_D from 0.2 Hz to 20 MHz, the results would have to be recalculated as follows:

1. $MTBF \approx 0.35 \text{ s (!)}$, which is completely useless.
2. $MTBF \approx 78 \text{ s (!)}$, which is also not applicable.
3. $MTBF \approx 16000 \text{ s}$, which is about 4.4 hours, which is also useless.

It would probably be necessary to further reduce the CLK frequency - here even a small reduction is significant due to the exponential dependence.

Improving the $MTBF$ by reducing the CLK frequency is effective, but it will reduce the overall speed of the system, as the clock pulses operate in other circuits as well. Then it is possible to go the way of expanding the sampler and include another trigger circuit behind the double sampler - a **triple sampler** is obtained. The $MTBF$ of the sampler created by the first and second trigger is then multiplied by the $MTBF$ of the sampler created by the second and third trigger, i.e. we get $MTBF^2$. This is usually a sufficiently large number even at a non-reduced CLK frequency. Regarding selecting the triggers, essential are parameters of Q1 and the requirements for Q2 are lower.

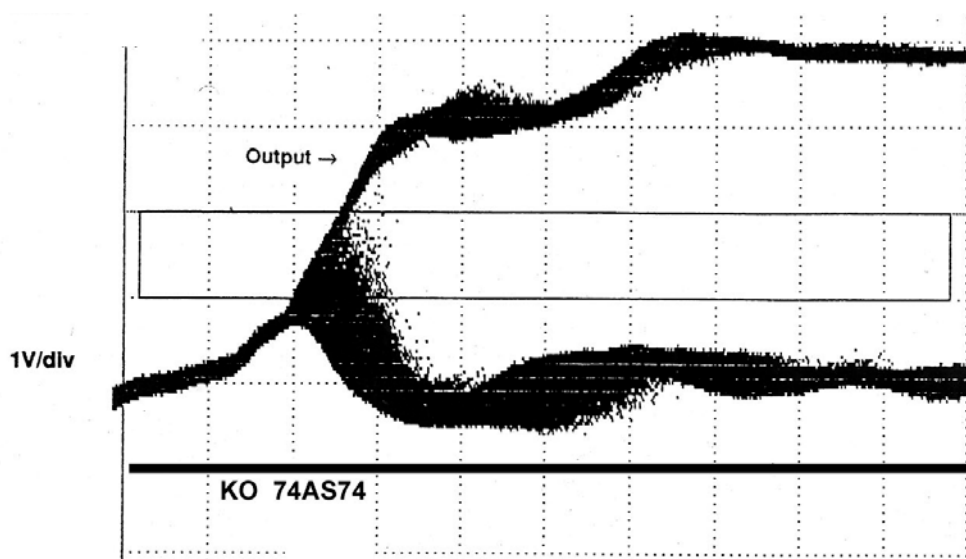


Fig. 21: Metastable trigger behavior